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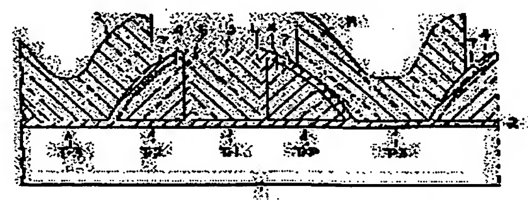
(54) SEMICONDUCTOR NONVOLATILE MEMORY AND ITS MANUFACTURE

(57)Abstract:
PURPOSE: To provide a semiconductor nonvolatile memory, which can be manufactured in high integration in terms of the existing processing technology and at low cost, and its manufacturing method.
CONSTITUTION: MONOS is used as a memory element. A first layer gate is thinned down by the resist ashing method. After an ONO film is formed, a transistor is made by a sidewall at a second layer which is a second polysilicon layer 4; then, the ONO film is formed to form a transistor between sidewalls in a third layer which is a third polysilicon layer 5. This enables the integration of a semiconductor nonvolatile memory to be improved.



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CLAIMS

[Claim(s)]
[Claim 1] A semiconductor nonvolatile storage which is a semiconductor nonvolatile storage which accumulates a charge in a gate insulator layer, and has 1st at least two storage element which set a predetermined gap and was formed, the 2nd storage element which makes the gate a sidewall of the gate section of the 1st storage element formed in a 1 side side through an interlayer film at least, and the 3rd storage element formed between the 2nd two storage element which set a predetermined gap.
[Claim 2] A semiconductor nonvolatile storage according to claim 1 which consists of insulator layers in which at least one side contains a nitriding insulator layer at least among interlayer films for separating between the above-mentioned gate insulator layer and an element.
[Claim 3] A semiconductor nonvolatile storage according to claim 1 or 2 with which a storage element is arranged by NAND mold.
[Claim 4] A semiconductor nonvolatile storage according to claim 1 or 2 with which a storage element is arranged by NOR mold of a contact loess mold.
[Claim 5] It is the manufacture method of a semiconductor nonvolatile storage which accumulates a charge in a gate insulator layer. After forming an insulator layer on a semiconductor substrate, the 1st polish recon is deposited on an insulator layer. If few, two storage elements which processed the 1st polish recon layer made to deposit by resist-ashing, and set a predetermined gap and which are the 1st will be formed. After forming an insulator layer in a substrate and the 1st storage element front face, the 2nd polish recon layer is formed in the at least 1 side of the 1st storage element. A manufacture method of a semiconductor nonvolatile storage characterized by forming the 3rd polish recon layer between the two 2nd polish recon layers which set a predetermined gap at least after forming an insulator layer in a front face of the 2nd polish recon layer at least.
[Claim 6] A manufacture method of a semiconductor nonvolatile storage according to claim 5 of forming the 3rd polish recon layer on the 1st and 2nd polish recon layers at a substrate and a list, embedding mask material in self align in a slot made after the 3rd polish recon stratification, and processing the 3rd polish recon layer by making this into a mask.

[Translation done.]

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Industrial Application] This invention relates to a semiconductor nonvolatile storage and its manufacture methods, such as rewritable nonvolatile memory, for example, a flash EEPROM etc., electrically.
[0002]
[Description of the Prior Art] Since information is saved even if it turns off the power, it is easy to use nonvolatile memory, and it is expanding a commercial scene. It roughly divides into arrangement of such a non-volatile memory cell, and there are a NOR mold and a NAND mold in it.
[0003] Drawing 6 is drawing showing the example of a configuration of a NOR mold non-volatile memory cell. It sets to drawing 6 and they are BL1 and BL2. A bit line, WL1, and WL2 A word line, and MT11, MT12, MT21 and MT22 show the memory cell transistor, respectively. As shown in drawing 6 , one bit contact CNTBL is shared between the transistor MT 11 of two ******, and MT12, MT21 and MT22. That is, 0.5 bit contacts CNTBL of per one transistor (1 bit) are needed.
[0004] Since such NOR mold nonvolatile memory of a configuration can carry out direct access, without minding other transistors, it is suitable for high-speed operation, but since per bit needs 0.5 to be contacted, it is difficult for it to raise a degree of integration.
[0005] On the other hand, NAND mold nonvolatile memory is the memory cell transistor MT 1 of plurality [between / the bit contact CNTBL and touch-down] - MT8, as shown in drawing 7 . It connects with the serial. In practice, although a selection transistor is inserted between a memory cell transistor, the bit contact CNTBL, and a gland, the bit contact CNTBL is shared also with an adjoining serial memory cell transistor group. Therefore, in the case of 8 bit-serial cel, it ends with one piece to 2= total (8+2) x20 transistor.
[0006] Since contact can be managed with one piece to the memory cell by which such NAND mold nonvolatile memory of a configuration was connected to the serial, although it is suitable for high integration, since other transistors are connected to the transistor to access at the serial, high-speed operation cannot use it for a required use.
[0007] Then, although rapidity is not required so much, when large capacity is required, it is made promising [NAND mold nonvolatile memory] for replacement and fixed tape of a hard disk. When used for this kind of use, since it is generally used widely that a price is low, it is very important. Since the number of bits per unit price area is larger than NOR mold nonvolatile memory, NAND mold nonvolatile memory is advantageous in cost, and has turned to this kind of use also in that semantics.
[0008]
[Problem(s) to be Solved by the Invention] However, although it is necessary to advance detailed-ization in order to raise a degree of integration further with the usual NAND structure, it is limited only by using the present processing technology. Moreover, in order to develop the new ultra-fine processing technology for it, it is accompanied by difficulty in time, technical, and cost.
[0009] It is in offering the semiconductor nonvolatile storage which this invention can be made in view of this situation, and the object can attain high integration within the limits of the present processing technology, as a result can attain low-pricing, and its manufacture method.
[0010]
[Means for Solving the Problem] In order to attain the above-mentioned object, a semiconductor nonvolatile storage which accumulates a charge in a gate insulator layer of this invention 1st at least two storage element which set a predetermined gap and was formed, and the 2nd storage element which makes the gate a sidewall of the gate section of the 1st storage element formed in a 1 side side through an interlayer film at least, It has the 3rd storage element formed

between the 2nd two storage element which set a predetermined gap.

[0011] Moreover, a semiconductor nonvolatile storage of this invention consists of insulator layers in which at least one side contains a nitriding insulator layer at least among interlayer films for separating between the above-mentioned gate insulator layer and an element.

[0012] Moreover, a storage element is arranged by NOR mold of a NAND mold or a contact loess mold in a semiconductor nonvolatile storage of this invention.

[0013] moreover, by manufacture method of a semiconductor nonvolatile storage which accumulates a charge in a gate insulator layer of this invention After forming an insulator layer on a semiconductor substrate, the 1st polish recon is deposited on an insulator layer. If few, two storage elements which processed the 1st polish recon layer made to deposit by resist-ashing, and set a predetermined gap and which are the 1st will be formed. After forming an insulator layer in a substrate and the 1st storage element front face, the 2nd polish recon layer is formed in the at least 1 side of the 1st storage element. After forming an insulator layer in a front face of the 2nd polish recon layer at least, the 3rd polish recon layer is formed between the two 2nd polish recon layers which set a predetermined gap at least.

[0014] Moreover, by manufacture method of a semiconductor nonvolatile storage of this invention, the 3rd polish recon layer is formed on the 1st and 2nd polish recon layers at a substrate and a list, mask material is embedded in self align in a slot made after the 3rd polish recon stratification, and the 3rd polish recon layer is processed on it by making this into a mask.

[0015]

[Function] According to the semiconductor nonvolatile storage of this invention, the degree of integration of a semiconductor nonvolatile storage improves by 4 times within the limits of the present processing technology.

[0016] Moreover, according to the manufacture method of this invention, first, after an insulator layer is formed on a semiconductor substrate, the 1st polish recon accumulates on an insulator layer. As for the deposited 1st polish recon layer, the width of face is processed using the resist-ashing method. Thereby, if few, two storage elements which set the predetermined gap and which are the 1st will be formed. Next, after an insulator layer is formed in a substrate and the 1st storage element front face, the 2nd polish recon layer is formed in the at least 1 side of the 1st storage element, and the 2nd storage element is constituted. Subsequently, after an insulator layer is formed in the front face of the 2nd polish recon layer at least, the 3rd polish recon layer is formed between the two 2nd polish recon layers which set the predetermined gap at least, and the 3rd storage element is constituted.

[0017] Moreover, according to this invention, the 3rd polish recon layer is formed on the 1st and 2nd polish recon layers at a substrate and a list. At this time, a slot is made in the 3rd polish recon layer formed between the 2nd polish recon layers. Mask material is embedded in self align in the slot made after this 3rd polish recon stratification, and it is processed on it so that the 3rd polish recon layer may be located between the two 2nd polish recon layers by making this into a mask.

[0018]

[Example] Drawing 1 is the cross section showing one example of the NAND mold semiconductor nonvolatile storage concerning this invention. drawing 1 -- setting -- Tr1 -- the 1st transistor and Tr2 -- the 2nd transistor and Tr3 -- the 3rd transistor and 1 -- in the 1st polish recon layer and 4, the 2nd polish recon layer and 5 show six, and, as for a semiconductor substrate and 2, the 3rd polish recon layer and 7 show [a gate insulator layer and 3] the interlayer insulation film, respectively.

[0019] The 1st transistor Tr1 is the so-called MONOS mold transistor from which the gate was constituted by the 1st polish recon layer 3. That is, the gate insulator layer of an MOS transistor is SiO2 / SiN/SiO2, as shown in drawing 2 . It is the memory transistor constituted by the ONO insulator layer which consists of three layers.

[0020] The 2nd transistor Tr2 is a MONOS mold transistor from which the gate was constituted by the 2nd polish recon layer 4. The 2nd polish recon layer 4 which constitutes the gate is formed in the both sides of the 1st polish recon layer 3 as the so-called sidewall through the interlayer insulation film 6.

[0021] The 2nd transistor Tr3 is a MONOS mold transistor from which the gate was constituted by the 3rd polish recon layer 5. The 3rd polish recon layer 5 is formed on the interlayer insulation film 7 formed at the list on the 1st polish recon layer 3 and the 2nd polish recon 4 on the gate insulator layer 2 between the 2nd adjoining transistor Tr2.

[0022] Thus, in this example, it is used as a gate insulator layer of the 1st - the 3rd transistor Tr1, Tr2, and Tr3, and the ONO film which has structure as shown in drawing 2 also has a function as an interlayer insulation film between each transistor, while being used for holding a memory function. In this case, although obtained by oxidizing polish recon, since the oxide film on polish recon has the property which becomes thicker than the substrate 1 top which consists of single crystal silicon, the oxide film (referred to also as Bottom Ox) of the lowest layer of ONO is suitable for the object of layer insulation.

[0023] Next, the manufacture method of the semiconductor nonvolatile storage of drawing 1 is explained, referring to drawing 3 . In addition, explanation of processes, such as an ion implantation without the direct relation to a configuration, is omitted.
[0024] First, phosphorus is doped, after forming the ONO film used as the gate insulator layer 2 on a substrate 1 and depositing the polish recon Poly in about 250nm thickness with a CVD method, as shown in drawing 3 (a). In addition, the thickness of the gate insulator layer 2 is SiO2 of the lowest layer of for example, an ONO film. For thickness, the thickness of 2nm and middle SiN is SiO2 of 4nm and the maximum upper layer. Thickness is set as 3nm.
[0025] Next, as shown in drawing 3 (b), patterning of the line/the space of the minimum design rule (last shipment) is carried out by Resist PR by the technique of lithography. A pattern gap is set as about 0.4 micrometers.
[0026] Next, as shown in drawing 3 (c), using the resist-ashing method, Resist PR is etched isotropic in the oxygen plasma, and resist line breadth is dwindled to about 0.2 micrometers. Under the present circumstances, it takes into consideration and the gate length of the 1st - the 3rd transistor Tr1, Tr2, and Tr3 determines that the amount to dwindle will become the same eventually. Thereby, the distance between adjoining resist patterns is set to about 0.6 micrometers. As concrete conditions for the resist-ashing method, it is set as power 100W, pressure 200mTorr, and oxygen gas 20SCCM.
[0027] Subsequently, a resist is exfoliated after RIE removes polish recon and an ONO film, as shown in drawing 3 (d). Next, as shown in drawing 3 (e), an ONO film is formed on a substrate 1 and a pattern. At this time, the ONO film on a substrate 1 is formed so that it may become the same thickness as the ONO film of the 1st transistor Tr1, but as mentioned above, the ONO film of the side of the 1st transistor Tr1 and the upper surface becomes thicker than a substrate 1 top. This is because a bottom product (Bottom) Ox becomes thick on polish recon, as mentioned above.
[0028] Next, as shown in drawing 4 (f), after forming the 2nd polish recon layer 4 with a CVD method and doping phosphorus, etchback is carried out by RIE and the sidewall of the 2nd polish recon layer 4 is formed. In this case, the ONO film of the field on the substrate 1 with which the 3rd transistor Tr3 is formed later is removed in the field in which the 1st polish recon layer 3 and the 2nd polish recon layer 4 are not formed. Therefore, most ONO films of the upper surface of the 1st transistor Tr1 are removed.
[0029] Next, as shown in drawing 4 (g), an ONO film is formed on a substrate 1, the 1st polish recon layer 3, and the 2nd polish recon layer 4. It forms so that the ONO film on a substrate 1 may serve as the same thickness as the ONO film of the 1st transistor Tr1 and the 2nd transistor Tr2 at this time, but as mentioned above, the ONO film of the upper surface of the 1st transistor Tr1 and the upper surface of the 2nd transistor Tr2 becomes thicker than a substrate 1 top.
[0030] Next, phosphorus is doped after forming 3rd polish recon layer 3P oly (5) with a CVD method on the whole ONO film, as shown in drawing 4 (h). Next, as shown in drawing 4 (i), patterning is carried out with lithography. The space at this time is good at the minimum interval of a design rule, and does not need to take a doubling gap margin. It is because a sidewall can be substituted for a doubling gap margin. And as shown in drawing 4 (j), the polish recon layer on the transistor Tr2 located in the 1st transistor Tr1 and the 1st about one transistor Tr field by RIE is removed [2nd], and a resist film is exfoliated. Hereafter, it progresses to processes, such as formation of an interlayer insulation film.
[0031] Moreover, the mask material 2, for example, SiO, SOG, or a resist is embedded in self align in the slot made instead of drawing 4 (i) and the process of (j) which were mentioned above when the 3rd polish recon layer 5 was formed by drawing 4 (h), and you may make it process the 3rd polish recon layer 5 on it by making it into a mask.
[0032] Next, it considers how many memory transistors can be formed into the line/space of one unit as a result using drawing 5 . In addition, in drawing 4 , L shows the minimum design rule, and since it is easy, it makes the line/space the length of 4L/4L. Moreover, the thickness of ONO has ignored.
[0033] As shown in drawing 5 (a), in the case of the usual 1st polish recon, the number of memory transistors is one in a line / space 1 unit. On the other hand, in this example, as shown in drawing 5 (b), four transistors of gate length 2L are formed into 4L+4L=8L. The 1st transistor Tr1 becomes one piece and two 2nd transistor Tr2 GA, and, specifically, the 3rd transistor Tr3 becomes one piece [a total of four]. Consequently, according to this example, a degree of integration can be increased 4 usual times.
[0034] As explained above, according to this example, MONOS is used as an element. After dwindling the gate of the 1st layer by the resist-ashing method and forming an ONO film, Since the transistor by the sidewall was produced by the 2nd polish recon 4 of a two-layer eye, the ONO film was formed further and the transistor was formed between sidewalls in the layer [3rd] 3rd polish recon layer 5 The degree of integration of nonvolatile memory can be improved within the limits of the present processing technology. Consequently, since the cost per bit can be reduced, there is an advantage -- the price of a product can be lowered. Moreover, it can double by the sidewall, a gap margin can be absorbed, and a memory cell can be formed using the minimum processing size.
[0035] In addition, at this example, although the NAND mold semiconductor nonvolatile storage was explained to the

example, it cannot be overemphasized that it is not limited to this and this invention can be applied also to the NOR semiconductor nonvolatile storage of a contact loess mold.

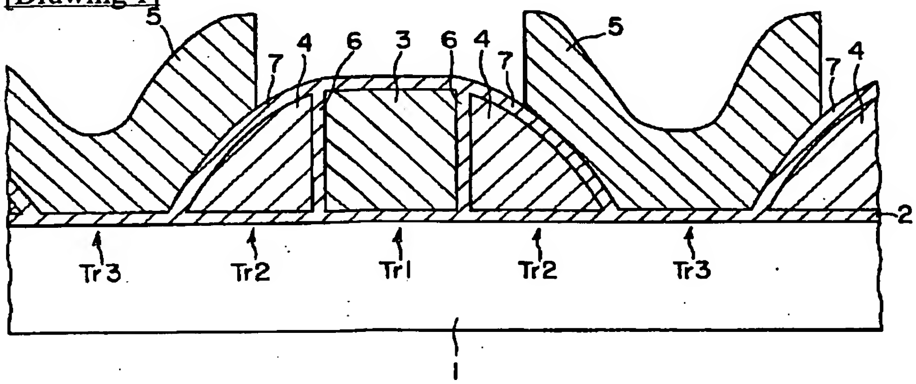
[0036]

[Effect of the Invention] As explained above, according to this invention, the degree of integration of nonvolatile memory can be improved within the limits of the present processing technology. Consequently, since the cost per bit can be reduced, there is an advantage -- the price of a product can be lowered.

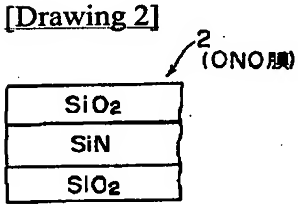
[Translation done.]

DRAWINGS

[Drawing 1]

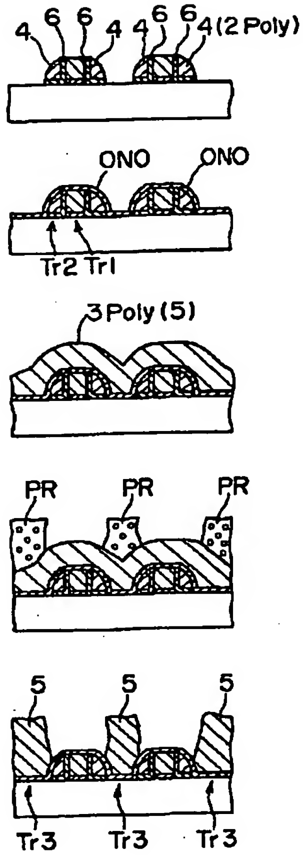


[Drawing 2]

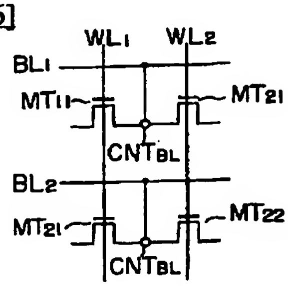


[Drawing 4]

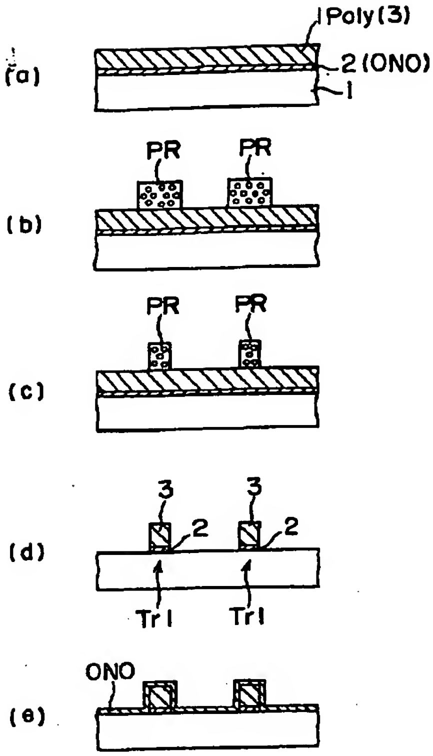
(f)
(g)
(h)
(i)
(j)



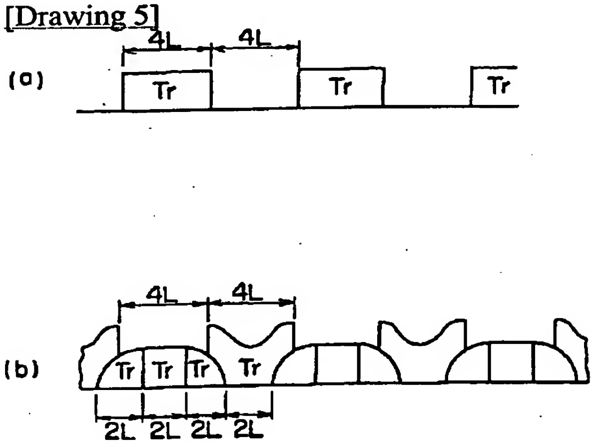
[Drawing 6]



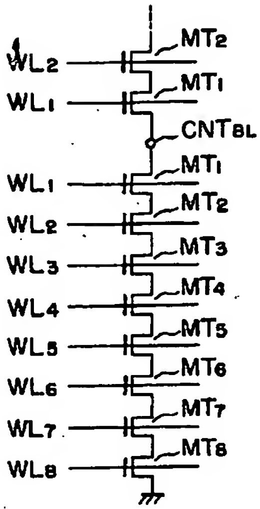
[Drawing 3]



[Drawing 5]



[Drawing 7]



[Translation done.]

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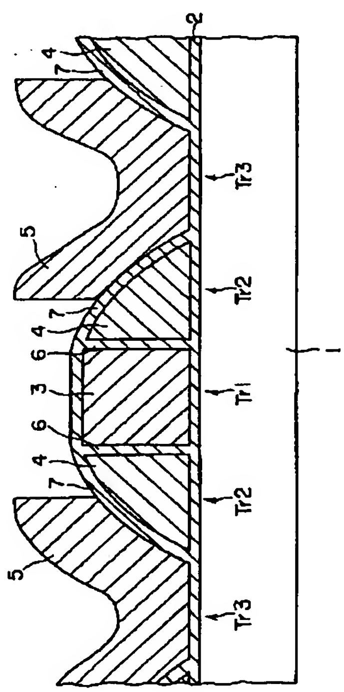
(54)【発明の名称】　半導体不揮発性記憶装置およびその製造方法

(57)【要約】

【目的】現行の加工技術の範囲内で、高集積化を図れ、ひいては低価格化を図れる半導体不揮発性記憶装置およびその製造方法を提供することにある。

【構成】　記憶素子としてはＭＯＮＯＳを使用し、１層目のゲートをレジストアッシング法で細らせ、ＯＮＯ膜を形成した後、２層目の第２ポリシリコン層４でサイドウォールによるトランジスタを作製し、さらにＯＮＯ膜を形成し、３層目の第３ポリシリコン層５でサイドウォール間にトランジスタを形成する。これにより、現行の加工技術の範囲内で、半導体不揮発性記憶装置の集積度の向上を図れる。



【特許請求の範囲】

【請求項１】　ゲート絶縁膜に電荷を蓄積する半導体不揮発性記憶装置であって、
所定間隔をおいて形成された少なくとも２つの第１の記憶素子と、
第１の記憶素子のゲート部の少なくとも一側面側に層間膜を介して形成されたサイドウォールをゲートとする第２の記憶素子と、
所定間隔をおいた２つの第２の記憶素子間に形成された第３の記憶素子とを有する半導体不揮発性記憶装置。

【請求項２】　上記ゲート絶縁膜および素子間を分離するための層間膜のうち少なくとも一方が、少なくとも窒化絶縁膜を含む絶縁膜から構成されている請求項１記載の半導体不揮発性記憶装置。

【請求項３】　記憶素子がＮＡＮＤ型に配列されている請求項１または請求項２記載の半導体不揮発性記憶装置。

【請求項４】　記憶素子がコンタクトレス型のＮＯＲ型に配列されている請求項１または請求項２記載の半導体不揮発性記憶装置。

【請求項５】　ゲート絶縁膜に電荷を蓄積する半導体不揮発性記憶装置の製造方法であって、
半導体基板上に絶縁膜を形成した後、
絶縁膜上に第１ポリシリコンを堆積し、
堆積させた第１ポリシリコン層をレジストアッシングにより加工して所定間隔をおいた少なくと２つの第１の記憶素子を形成し、
基板および第１の記憶素子表面に絶縁膜を形成した後、
第１の記憶素子の少なくとも一側に第２ポリシリコン層を形成し、
少なくとも第２ポリシリコン層の表面に絶縁膜を形成した後、
少なくとも所定間隔をおいた２つの第２ポリシリコン層間に第３ポリシリコン層を形成することを特徴とする半導体不揮発性記憶装置の製造方法。

【請求項６】　第３ポリシリコン層を基板、並びに第１および第２のポリシリコン層上に形成し、第３ポリシリコン層形成後にできた溝に、マスク材を自己整合的に埋め込み、これをマスクとして第３ポリシリコン層を加工する請求項５記載の半導体不揮発性記憶装置の製造方法。

【発明の詳細な説明】

【０００１】

【産業上の利用分野】本発明は、電気的に書き換え可能な不揮発性メモリ、たとえばフラッシュＥＥＰＲＯＭなどの半導体不揮発性記憶装置およびその製造方法に関するものである。

【０００２】

【従来の技術】不揮発性メモリは電源を切っても情報が保存されるため使いやすく、市場を拡大しつつある。このような不揮発性メモリセルの配置には、大きく分けてＮＯＲ型とＮＡＮＤ型がある。

【０００３】図６は、ＮＯＲ型不揮発性メモリセルの構成例を示す図である。図６において、BL_1，BL_2 はビット線、WL_1，WL_2 はワード線、MT_{11}，MT_{12}，MT_{21}，MT_{22}はメモリセルトランジスタをそれぞれ示している。図６に示すように、隣合う２つのトランジスタMT_{11}およびMT_{12}、MT_{21}およびMT_{22}で、ビットコンタクトCNT_{BL}を１個共有する。すなわち、１トランジスタ（１ビット）当りのビットコンタクトCNT_{BL}を０．５個必要とする。

【０００４】このような構成のＮＯＲ型不揮発性メモリは、他のトランジスタを介さずに直接アクセスできることから高速動作に適しているが、１ビット当りのコンタクトが０．５個必要なため集積度を上げるのが難しい。

【０００５】これに対して、ＮＡＮＤ型不揮発性メモリは、図７に示すように、ビットコンタクトCNT_{BL}と接地との間に複数のメモリセルトランジスタMT_1 ～MT_8 が直列に接続されている。実際は、メモリセルトランジスタとビットコンタクトCNT_{BL}およびグランド間に選択トランジスタが挿入されるが、ビットコンタクトCNT_{BL}は隣接する直列メモリセルトランジスタ群とも共有する。したがって、８ビット直列セルの場合、計（８＋２）×２＝２０トランジスタに１個で済む。

【０００６】このような構成のＮＡＮＤ型不揮発性メモリは、直列に接続されたメモリセルに対し、コンタクトは１個で済むので高集積化には適しているものの、アクセスしたいトランジスタに直列に他のトランジスタが接続されていることから、高速動作が必要な用途には使用できない。

【０００７】そこで、高速性はそれほど要求しないが大容量が必要な場合、たとえばハードディスクの置き換えや固定テープにはＮＡＮＤ型不揮発性メモリが有望とされている。この種の用途に用いられる場合は、価格が低いことが一般に広く用いられるために極めて重要である。ＮＡＮＤ型不揮発性メモリは、単価面積当りのビット数がＮＯＲ型不揮発性メモリより大きいので、コスト的に有利であり、その意味でもこの種の用途に向いている。

【０００８】

【発明が解決しようとする課題】しかしながら、通常のＮＡＮＤ構造のままでさらに集積度を向上させるには、微細化を進める必要があるが、それは現行の加工技術を用いるだけでは限度がある。また、そのための新しい微細加工技術を開発するために、時間的・技術的・コスト的に困難を伴う。

【０００９】本発明は、かかる事情に鑑みてなされたものであり、その目的は、現行の加工技術の範囲内で、高集積化を図れ、ひいては低価格化を図れる半導体不揮発性記憶装置およびその製造方法を提供することにある。

【００１０】

【課題を解決するための手段】上記目的を達成するため、本発明のゲート絶縁膜に電荷を蓄積する半導体不揮発性記憶装置は、所定間隔をおいて形成された少なくとも２つの第１の記憶素子と、第１の記憶素子のゲート部の少なくとも一側面側に層間膜を介して形成されたサイドウォールをゲートとする第２の記憶素子と、所定間隔をおいた２つの第２の記憶素子間に形成された第３の記憶素子とを有する。

【００１１】また、本発明の半導体不揮発性記憶装置は、上記ゲート絶縁膜および素子間を分離するための層間膜のうち少なくとも一方が、少なくとも窒化絶縁膜を含む絶縁膜から構成されている。

【００１２】また、本発明の半導体不揮発性記憶装置では、記憶素子がＮＡＮＤ型、あるいはコンタクトレス型のＮＯＲ型に配列される。

【００１３】また、本発明のゲート絶縁膜に電荷を蓄積する半導体不揮発性記憶装置の製造方法では、半導体基板上に絶縁膜を形成した後、絶縁膜上に第１ポリシリコンを堆積し、堆積させた第１ポリシリコン層をレジストアッシングにより加工して所定間隔をおいた少なくと２つの第１の記憶素子を形成し、基板および第１の記憶素子表面に絶縁膜を形成した後、第１の記憶素子の少なくとも一側に第２ポリシリコン層を形成し、少なくとも第２ポリシリコン層の表面に絶縁膜を形成した後、少なくとも所定間隔をおいた２つの第２ポリシリコン層間に第３ポリシリコン層を形成する。

【００１４】また、本発明の半導体不揮発性記憶装置の製造方法では、第３ポリシリコン層を基板、並びに第１および第２のポリシリコン層上に形成し、第３ポリシリコン層形成後にできた溝に、マスク材を自己整合的に埋め込み、これをマスクとして第３ポリシリコン層を加工する。

【００１５】

【作用】本発明の半導体不揮発性記憶装置によれば、現行の加工技術の範囲内で、半導体不揮発性記憶装置の集積度が４倍に向上する。

【００１６】また、本発明の製造方法によれば、まず、半導体基板上に絶縁膜が形成された後、絶縁膜上に第１ポリシリコンが堆積される。堆積された第１ポリシリコン層は、レジストアッシング法を用いてその幅が加工される。これにより、所定間隔をおいた少なくと２つの第１の記憶素子が形成される。次に、基板および第１の記憶素子表面に絶縁膜が形成された後、第１の記憶素子の少なくとも一側に第２ポリシリコン層が形成され、第２の記憶素子が構成される。次いで、少なくとも第２ポリシリコン層の表面に絶縁膜が形成された後、少なくとも所定間隔をおいた２つの第２ポリシリコン層間に第３ポリシリコン層が形成され、第３の記憶素子が構成される。

【００１７】また、本発明によれば、第３ポリシリコン層が基板、並びに第１および第２のポリシリコン層上に形成される。このとき、第２ポリシリコン層間に形成される第３ポリシリコン層には溝ができる。この第３ポリシリコン層形成後にできた溝に、マスク材が自己整合的に埋め込まれ、これをマスクとして第３ポリシリコン層が２つの第２ポリシリコン層間に位置するように加工される。

【００１８】

【実施例】図１は、本発明に係るＮＡＮＤ型半導体不揮発性記憶装置の一実施例を示す断面図である。図１において、Tr1は第１のトランジスタ、Tr2は第２のトランジスタ、Tr3は第３のトランジスタ、１は半導体基板、２はゲート絶縁膜、３は第１ポリシリコン層、４は第２ポリシリコン層、５は第３ポリシリコン層、６，７は層間絶縁膜をそれぞれ示している。

【００１９】第１のトランジスタTr1は、ゲートが第１ポリシリコン層３により構成された、いわゆるＭＯＮＯＳ型トランジスタである。すなわち、ＭＯＳトランジスタのゲート絶縁膜が、図２に示すように、SiO_2／SiN／SiO_2 の３層からなるＯＮＯ絶縁膜により構成されたメモリトランジスタである。

【００２０】第２のトランジスタTr2は、ゲートが第２ポリシリコン層４により構成されたＭＯＮＯＳ型トランジスタである。ゲートを構成する第２ポリシリコン層４は、第１ポリシリコン層３の両側に層間絶縁膜６を介し、いわゆるサイドウォールとして形成されている。

【００２１】第２のトランジスタTr3は、ゲートが第３ポリシリコン層５により構成されたＭＯＮＯＳ型トランジスタである。第３ポリシリコン層５は、隣接する第２のトランジスタTr2間のゲート絶縁膜２上、並びに第１ポリシリコン層３および第２ポリシリコン４上に形成された層間絶縁膜７上に形成されている。

【００２２】このように、本実施例においては、図２に示すような構造を有するＯＮＯ膜が、第１～第３のトランジスタTr1，Tr2，Tr3のゲート絶縁膜として用いられ、メモリ機能を保持するのに利用されると共に、各トランジスタ間の層間絶縁膜としての機能も持つ。この場合、ＯＮＯの最下層の酸化膜（Ｂｏｔｔｏｍ　Ｏｘとも呼ぶ）はポリシリコンを酸化することにより得られるが、ポリシリコン上の酸化膜は単結晶シリコンからなる基板１上より厚くなる性質があるので、層間絶縁の目的に好適である。

【００２３】次に、図３を参照しながら、図１の半導体不揮発性記憶装置の製造方法について説明する。なお、形状に直接関係のないイオン注入等の工程の説明は省略している。

【００２４】まず、図３（ａ）に示すように、基板１上にゲート絶縁膜２となるＯＮＯ膜を形成した後、ＣＶＤ法によりポリシリコンＰｏｌｙを２５０ｎｍ程度の膜厚

で堆積した後、燐をドーピングする。なお、ゲート絶縁膜２の膜厚は、たとえば、ＯＮＯ膜の最下層のSiO_2の膜厚は２ｎｍ、中間のＳｉＮの膜厚は４ｎｍ、最上層のSiO_2の膜厚は３ｎｍに設定する。

【００２５】次に、図３（ｂ）に示すように、リソグラフィーの手法により最小のデザインルールのライン／スペース（Ｌ／Ｓ）をレジストＰＲでパターニングする。パターン間隔は、たとえば０．４μｍ程度に設定する。

【００２６】次に、図３（ｃ）に示すように、レジストアッシング法を用い、酸素プラズマ中でレジストＰＲを等方的にエッチングし、レジスト線幅を０．２μｍ程度に細らせる。この際、細らせる量は第１～第３のトランジスタTr1，Tr2，Tr3のゲート長が最終的に同じになるように考慮して決定する。これにより、隣接するレジストパターン間の距離は、０．６μｍ程度となる。レジストアッシング法の具体的な条件としては、パワー１００Ｗ、圧力２００ｍＴｏｒｒ、酸素ガス２０ＳＣＣＭに設定する。

【００２７】次いで、図３（ｄ）に示すように、ＲＩＥによりポリシリコンおよびＯＮＯ膜を除去した後、レジストを剥離する。次に、図３（ｅ）に示すように、基板１およびパターン上にＯＮＯ膜を形成する。このとき、基板１上のＯＮＯ膜は第１のトランジスタTr1のＯＮＯ膜と同じ膜厚になるように形成するが、前述したように、第１のトランジスタTr1の側面と上面のＯＮＯ膜は基板１上より厚くなる。これは、上述したように、ボトム（Ｂｏｔｔｏｍ）Ｏｘがポリシリコン上で厚くなるためである。

【００２８】次に、図４（ｆ）に示すように、ＣＶＤ法により第２ポリシリコン層４を形成し、燐をドーピングした後、ＲＩＥでエッチバックし第２ポリシリコン層４のサイドウォールを形成する。この場合、第１ポリシリコン層３および第２ポリシリコン層４が形成されていない領域で、後で第３のトランジスタTr3が形成される基板１上の領域のＯＮＯ膜を除去する。そのため、第１のトランジスタTr1の上面のＯＮＯ膜もほとんど除去される。

【００２９】次に、図４（ｇ）に示すように、基板１、第１ポリシリコン層３および第２ポリシリコン層４上にＯＮＯ膜を形成する。このとき、基板１上のＯＮＯ膜は、第１のトランジスタTr1および第２のトランジスタTr2のＯＮＯ膜と同じ膜厚となるように形成するが、上述したように、第１のトランジスタTr1の上面と第２のトランジスタTr2の上面のＯＮＯ膜は、基板１上より厚くなる。

【００３０】次に、図４（ｈ）に示すように、全体のＯＮＯ膜上にＣＶＤ法により第３ポリシリコン層３Ｐｏｌｙ（５）を形成した後、燐をドーピングする。次に、図４（ｉ）に示すように、リソグラフィーによりパターニングする。このときのスペースはデザインルールの最小間隔で良く、合わせずれマージンを取らなくてよい。合わせずれマージンはサイドウォールで代用できるからである。そして、図４（ｊ）に示すように、ＲＩＥで第１のトランジスタTr1および第１のトランジスタTr1近傍領域に位置する第２にトランジスタTr2上のポリシリコン層を除去し、レジスト膜を剥離する。以下、層間絶縁膜の形成等の工程に進む。

【００３１】また、上述した図４（ｉ）および（ｊ）の工程の代わりに、たとえば図４（ｈ）で第３ポリシリコン層５を形成したときにできた溝に、マスク材、たとえばSiO_2、ＳＯＧあるいはレジストを自己整合的に埋め込み、それをマスクとして第３ポリシリコン層５を加工するようにしてもよい。

【００３２】次に、図５を用いて結果的に１単位のライン／スペースの中に幾つのメモリトランジスタを形成可能であるかを考察する。なお、図４において、Ｌは最小デザインルールを示しており、簡単のためライン／スペースを４Ｌ／４Ｌの長さとしている。また、ＯＮＯの膜厚は無視している。

【００３３】図５（ａ）に示すように、通常の第１ポリシリコンの場合は、ライン／スペース１単位でメモリトランジスタは１個だけである。これに対して、本実施例では、図５（ｂ）に示すように、４Ｌ＋４Ｌ＝８Ｌの中に、ゲート長２Ｌのトランジスタが４つ形成される。具体的には、第１のトランジスタTr1が１個、第２トランジスタTr2ガ２個、第３のトランジスタTr3が１個の計４個となる。その結果、本実施例によれば、集積度を通常の４倍にすることができる。

【００３４】以上説明したように、本実施例によれば、素子としてはＭＯＮＯＳを使用し、１層目のゲートをレジストアッシング法で細らせ、ＯＮＯ膜を形成した後、２層目の第２ポリシリコン４でサイドウォールによるトランジスタを作製し、さらにＯＮＯ膜を形成し、３層目の第３ポリシリコン層５でサイドウォール間にトランジスタを形成したので、現行の加工技術の範囲内で、不揮発性メモリの集積度を向上することができる。その結果、ビット当りのコストを低減することができることから、製品の価格を下げられる等の利点がある。また、サイドウォールにより合わせずれマージンを吸収し、最小加工寸法を用いてメモリセルを形成することができる。

【００３５】なお、本実施例では、ＮＡＮＤ型半導体不揮発性記憶装置を例に説明したが、これに限定されるものではなく、たとえばコンタクトレス型のＮＯＲ半導体不揮発性記憶装置にも本発明が適用できることはいうまでもない。

【００３６】

【発明の効果】以上説明したように、本発明によれば、現行の加工技術の範囲内で、不揮発性メモリの集積度を向上することができる。その結果、ビット当りのコストを低減することができることから、製品の価格を下げら

れる等の利点がある。

【図面の簡単な説明】

【図１】本発明に係るＮＡＮＤ型半導体不揮発性記憶装置の一実施例を示す断面図である。

【図２】ＯＮＯ構造の説明図である。

【図３】図１の半導体不揮発性記憶装置の製造方法を説明するための図である。

【図４】図１の半導体不揮発性記憶装置の製造方法を説明するための図である。

【図５】本発明品と従来品との集積度を比較、説明するための図である。

【図６】ＮＯＲ型メモリセルを説明するための図である。

【図７】ＮＡＮＤ型メモリセルを説明するための図である。

【符号の説明】

Ｔｒ1…第１のトランジスタ

Ｔｒ2…第２のトランジスタ

Ｔｒ3…第３のトランジスタ

１…半導体基板

２…ゲート絶縁膜

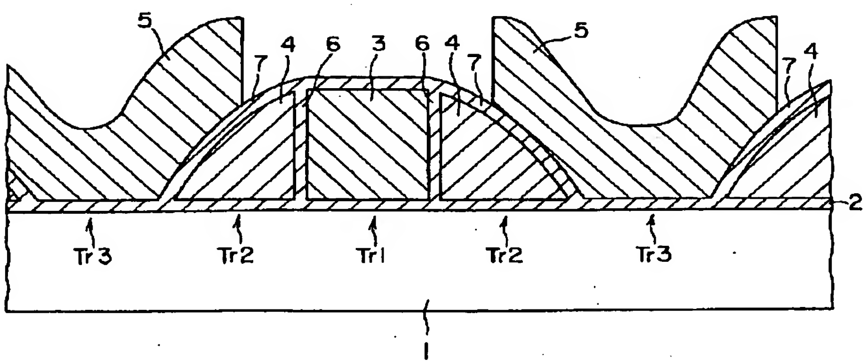
３…第１ポリシリコン層

４…第２ポリシリコン層

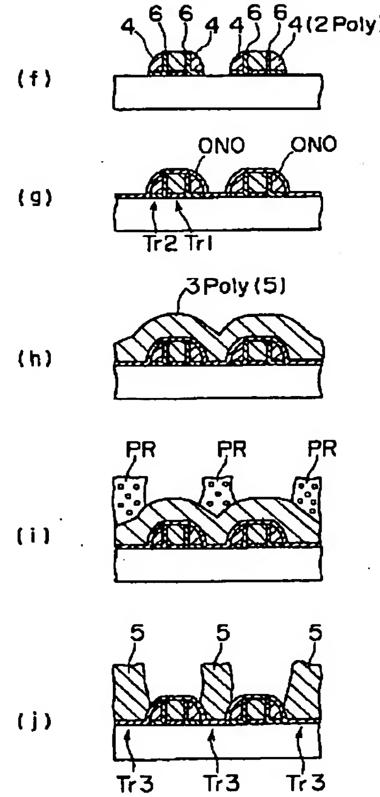
５…第３ポリシリコン層

６，７…層間絶縁膜

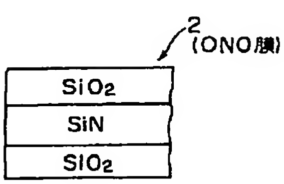
【図１】



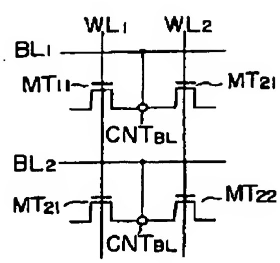
【図４】



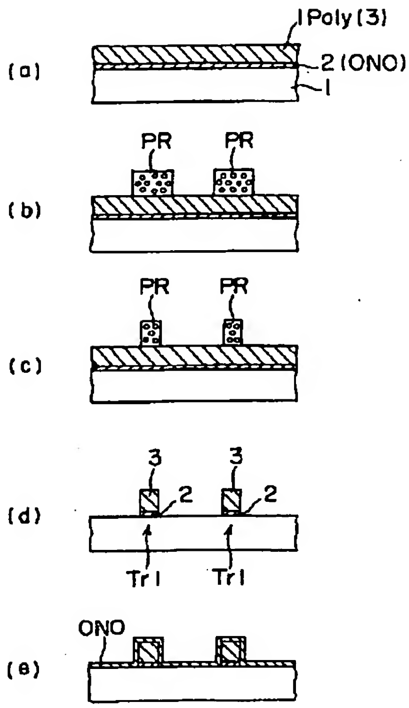
【図２】



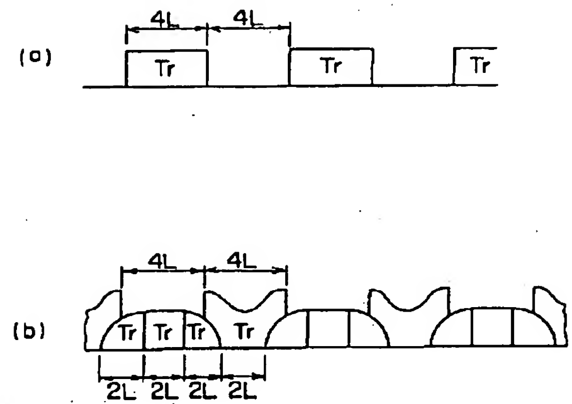
【図６】



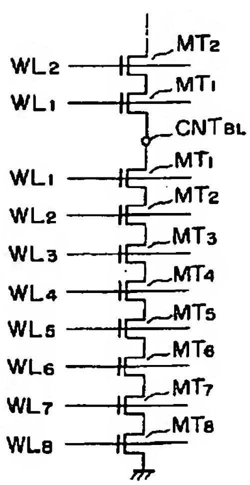
【図3】


Poly (3)
2 (ONO)
1
(a)
(b)
(c)
(d)
(e)
PR
3
2
Tr1
ONO

【図5】


(a)
(b)
4L
Tr
2L

【図7】


WL2
WL1
MT2
MT1
CNTBL
WL3
WL4
WL5
WL6
WL7
WL8
MT3
MT4
MT5
MT6
MT7
MT8

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(54) SEMICONDUCTOR NONVOLATILE MEMORY AND ITS MANUFACTURE

(57) Abstract: PURPOSE: To provide a semiconductor nonvolatile memory, which can be manufactured in high integration in terms of the existing processing technology and at low cost, and its manufacturing method. CONSTITUTION: MONOS is used as a memory element. A first layer gate is thinned down by the resist ashing method. After an ONO film is formed, a transistor is made by a sidewall at a second layer which is a second polysilicon layer 4; then, the ONO film is formed to form a transistor between sidewalls in a third layer which is a third polysilicon layer 5. This enables the integration of a semiconductor nonvolatile memory to be improved.

[Claim(s)]

[Claim 1] The semiconductor nonvolatile storage which accumulates a charge to a gate insulator layer, which has at least

two 1st storage elements formed setting a predetermined spacing

the 2nd storage element which makes the side wall the gate formed on at least the 1 side-face side of the gate section of the 1st storage element through the layer inbetween, and

the 3rd storage element formed between the 2nd two storage elements which set the predetermined spacing.

[Claim 2] The semiconductor nonvolatile storage according to claim 1 in which at least

one side is constituted from an insulator layer which contains a nitriding insulator layer at least among the layer inbetween for separating between the above-mentioned gate insulator layer and an element.

[Claim 3] The semiconductor nonvolatile storage according to claim 1 or 2 in which the storage element is arranged as NAND type.

[Claim 4] The semiconductor nonvolatile storage according to claim 1 or 2 in which the storage element is arranged as contact less type NOR type.

[Claim 5] A manufacture technique of the semiconductor nonvolatile storage which accumulates a charge to a gate insulator layer, and is characterized by the following:

After forming an insulator layer on a semiconductor substrate, the 1st polysilicon is deposited on said insulator layer, the deposited 1st polysilicon layer is processed by resist-ashing, and the predetermined spacing is set and at least two first storage elements are formed,

after forming an insulator layer on the substrate and the 1st storage element front face, a 2nd polysilicon layer is formed on at least one of the sides of the 1st storage element, and

after forming an insulator layer on the front face of the 2nd polysilicon layer at least, between the at least two 2nd polysilicon layers which are set at a predetermined spacing the 3rd polysilicon layer is formed.

[Claim 6] The manufacture technique of the semiconductor nonvolatile storage according to claim 5, in which

the 3rd polysilicon layer is formed on the substrate, the 1st, and the 2nd polysilicon layers,

in the groove created by the 3rd polysilicon layer forming, mask material is self-adjustingly applied, and with this as a mask the 3rd polysilicon layer is formed.

[Detailed Description of the Invention]

[0001]

[Field of the Invention] This invention relates to a semiconductor nonvolatile storage and its manufacture technique, such as an electrically rewritable non-volatile memory, for example, a flash EEPROM etc.

[0002]

[Description of the Prior Art] Since the information is saved even if the power is turned off, non-volatile memories are easy to use, and their market keeps expanding. They roughly divide into nonvolatile memory cell layouts of the NOR type and of the NAND type.

[0003] Fig. 6 is a drawing showing an example of a configuration of a NOR type nonvolatile memory cell. In Fig. 6, BL1, BL2 show bit lines, WL1, and WL2 show word lines, and MT11, MT12, MT21 and MT22 show memory cell transistors, respectively. As shown in Fig. 6, one bit contact CNTBL is shared between two adjacent transistors MT11 and MT12, MT21 and MT22. That is, 0.5 bit contact CNTBLs per one transistor (1 bit) are needed.

[0004] Although it is suitable for fast operation since such NOR type non-volatile memory of a configuration can be directly accessed without the mediation of other transistors, it is difficult to raise the degree of integration since every bit needs 0.5 contacts.

[0005] On the other hand, in the case of NAND type non-volatile memories, a plurality of memory cell transistors MT1 - MT8 are connected in series between the bit contacts CNTBL and the electrical grounding, as shown in Fig. 7.

In practice, although between a memory cell transistor and bit contact CNTBL and the ground, a selection transistor is inserted, the bit contact CNTBL shares an adjoining in-series memory cell transistor group.

Therefore, in the case of 8 bit-serial cells, one piece requires only a total of (8+2) x 2 = 20 transistors.

[0006] A NAND type non-volatile memory of such a configuration, compared to the memory cell which was connected in series, although since a contact can be managed with one piece it is suitable for high integration, since other transistors are connected to the transistor to be accessed in series, it cannot be used for required intended fast turn around use.

[0007] Then, NAND type non-volatile memory is promising when although rapidity is not demanded so much, but large capacity is required, for example for the displacement of a hard disk and fixed tape.

When used for this kind of intended use, since it is generally used widely, that price is low, it is very important.

Since the number of bits per unit price area is larger than NOR type non-volatile memory,

NAND type non-volatile memory is advantageous in cost, and in this respect too is advantageous for this kind of intended use.

[0008]

[Problem(s) to be Solved by the Invention] However, although it is necessary to advance micronization in order to raise a degree of integration further with usual NAND structure, it is limited if using only present processing technique.

Moreover, in order to develop the new micro-processing technique for it, it is accompanied by the distress in time, technical, and cost.

[0009] The purpose of this invention is to offer the semiconductor nonvolatile storage and its manufacture technique in view of such a situation, and to attain high integration within the limits of present processing techniques, and as a result to attain cost reduction.

[0010]

[Means for Solving the Problem] In order to attain the above-mentioned purpose, the semiconductor nonvolatile storage of this invention which accumulates a charge to the gate insulator layer has

at least two 1st storage element which was formed sets a predetermined spacing,

the 2nd storage element which uses as the gate the side wall formed on at least 1 side-face side of the gate section of the 1st storage element through the layer inbetween, and

the 3rd storage element formed between the two 2nd storage elements which set the predetermined spacing.

[0011] Moreover, the semiconductor nonvolatile storage of this invention consists of an insulator layer in which at least one side contains a nitriding insulator layer at least among the layer inbetween for separating between the above-mentioned gate insulator layer and an element.

[0012] Moreover, a storage element is arranged by NAND type or contact less type NOR type in the semiconductor nonvolatile storage of this invention.

[0013] Moreover, the manufacture technique of the semiconductor nonvolatile storage which accumulates a charge to the gate insulator layer of this invention includes the steps of

after forming an insulator layer on a semiconductor substrate, the 1st polysilicon is deposited on an insulator layer,

the 1st polysilicon layer made to deposit is processed by resist-ashing, and the at least two 1st storage elements are formed setting the predetermined spacing,

after forming an insulator layer on a substrate and the 1st storage element front face, the 2nd polysilicon layer is formed on at least 1 side of the 1st storage element,

after forming an insulator layer on the front face of the 2nd polysilicon layer at least, the 3rd polysilicon layer is formed between the at least two 2nd polysilicon layers which set the predetermined spacing.

[0014] Moreover, by the manufacture technique of the semiconductor nonvolatile storage of this invention, the 3rd polysilicon layer is formed on the substrate, the 1st, and 2nd polysilicon layers, and the 3rd polysilicon layer is processed into the slot made after the 3rd polysilicon stratification, embedding mask material on a self-matching target and using this as a mask.

[0015]

[Function] According to the semiconductor nonvolatile storage of this invention, the degree of integration of a semiconductor nonvolatile storage improves by 4 times within the limits of present manipulation technique.

[0016] Moreover, according to the manufacture technique of this invention,

first, after forming an insulator layer on a semiconductor substrate, the 1st polysilicon is accumulated on an insulator layer.

As for the deposited 1st polysilicon layer, the width of face is processed using the resist-ashing method.

Thereby the at least two 1st storage elements are formed at set predetermined spacing.

Next, after forming an insulator layer on a substrate and the 1st storage element front face, the 2nd polysilicon layer is formed in the at least 1 side of the 1st storage element, and the 2nd storage element is constituted.

Subsequently, after forming an insulator layer in the front face of the 2nd polysilicon layer at least, the 3rd polysilicon layer is formed between the at least two 2nd polysilicon layers which set the predetermined spacing, and the 3rd storage element is constituted.

[0017] Moreover, according to this invention, the 3rd polysilicon layer is formed on the substrate, the 1st, and 2nd polysilicon layers.

At this time, a slot is made in the 3rd polysilicon layer formed between the 2nd polysilicon layers.

In the slot made after this 3rd polysilicon stratification, mask material is embedded on a self-matching target and using this as a mask, the 3rd polysilicon layer is processed so that it may be located between the two 2nd polysilicon layers.

[0018]

[Embodiment] Fig. 1 is a cross section showing one embodiment of NAND type semiconductor nonvolatile storage concerning this invention.

In Fig. 1, Tr1 is the 1st transistor, Tr2 the 2nd transistor, Tr3 the 3rd transistor, 1 the

semiconductor substrate and 2 the gate insulator layer, 3 the 1st polysilicon layer, 4 the 2nd polysilicon layer, 5 the 3rd polysilicon layer and 6 and 7 show the inbetween layers insulation layer, respectively.

[0019] The 1st transistor Tr1 is the so-called MONOS type transistor from which the gate was constituted by the 1st polysilicon layer 3. That is, the gate insulator layer of an MOS transistor, as shown in Fig. 2 , is the memory transistor constituted by ONO insulator layers which consist of three SiO2/SiN/SiO2 layers.

[0020] The 2nd transistor Tr2 is a MONOS type transistor from which the gate was constituted by the 2nd polysilicon layer 4.

The 2nd polysilicon layer 4 which constitutes the gate is formed in the both sides of the 1st polysilicon layer 3, through the inbetween-layers insulation layer 6, as the side wall, that is.

[0021] The 2nd transistor Tr3 is MONOS type transistor from which the gate was constituted by the 3rd polysilicon layer 5.

The 3rd polysilicon layer 5 is formed on the layer insulation layer 7 formed on the 1st polysilicon layer 3 and the 2nd polysilicon 4 and on the gate insulator layer 2 between the adjoining 2nd transistors Tr2.

[0022] Thus, in this embodiment, the ONO layer which has the structure as shown in Fig. 2 is used as a gate insulator layer of the 1st to the 3rd transistor Tr1, Tr2, and Tr3, and while it is used for holding a memory function, it also has a function as a layer insulation layer between each transistor.

In this case, although the oxide film (referred to also as Bottom Ox) of the lowest layer of ONO is obtained by oxidizing polysilicon, since the oxide film on a polysilicon has the property of becoming thicker than the substrate 1 top which consists of single crystal silicon, it is suitable for the purpose of layer insulation.

[0023] Next, the manufacture technique of the semiconductor nonvolatile storage of Fig. 1 is explained, referring to Fig. 3.

In addition, the explanation of processes, such as an ion implantation without the direct relation to a configuration, is omitted.

[0024] First, phosphorus is doped, after forming ONO layer used as the gate insulator layer 2 on a substrate 1 and depositing polysilicon Poly by the about 250nm thickness by CVD, as shown in Fig. 3 (a).

In addition, the thickness of the gate insulator layer 2 is, for example, set by the thickness of the lowest SiO2 ONO layer of 2nm,

the thickness of the middle SiN layer of 4nm and
the thickness of the uppermost SiO2 layer of 3nm.

[0025] Next, as shown in Fig. 3 (b), patterning of the line / space of the minimum design rule (L/S) is carried out by resist PR by the technique of lithography.

A pattern spacing is set as about 0.4 micrometers.

[0026] Next, as shown in Fig. 3 (c), using the resist-ashing method, resist PR are etched isotropic in an oxygen plasma, and resist line breadth is dwindled to about 0.2 micrometers.

In this case, the amount to dwindle is determined taking into consideration that the gate length of the 1st to the 3rd transistor Tr1, Tr2, and Tr3 will finally become the same.

Thereby, the distance between adjoining resist patterns is set to about 0.6 micrometers.

As concrete conditions of the resist-ashing method, the power is set at 100W, pressure at 200mTorr, and oxygen gas at 20SCCM.

[0027] Subsequently, a resist is exfoliated, after removing polysilicon and ONO layer by RIE, as shown in Fig. 3 (d).

Next, as shown in Fig. 3 (e), ONO layer is formed on the substrate 1 and a pattern.

Although ONO layer on a substrate 1 is formed at this time so that it may become the same thickness as ONO layer of the 1st transistor Tr1,

as mentioned above, ONO layer of the side and top face of the 1st transistor Tr1 becomes thicker than on top of the substrate 1.

This is because a bottom Ox becomes thick on a polysilicon, as mentioned above.

[0028] Next, as shown in Fig. 4 (f), after forming the 2nd polysilicon layer 4 by CVD and doping phosphorus, etchback is carried out by RIE and the side wall of the 2nd polysilicon layer 4 is formed.

In this case, in the field in which the 1st polysilicon layer 3 and the 2nd polysilicon layer 4 is not formed, the field of the ONO layer of substrate 1 in which 3rd transistor Tr3 is formed is later removed.

Therefore, most of the ONO layers of the top of the 1st transistor Tr1 are removed.

[0029] Next, as shown in Fig. 4 (g), the ONO layer is formed on top of substrate 1, on top of the 1st polysilicon layer 3 and the 2nd polysilicon layer 4.

Although the ONO layer on top of substrate 1 is formed so as to have the same layer thickness as the ONO layer of the 1st polysilicon layer 3 and the 2nd polysilicon layer 4, as mentioned above, the ONO layer on top of the 1st transistor Tr1 and on top of the 2nd transistor Tr2 becomes thicker than on top of substrate 1.

[0030] Next, phosphorus is doped, after forming 3rd polysilicon layer 3 Poly (5) by CVD on the whole ONO layer, as shown in Fig. 4 (h).

Next, as shown in Fig. 4 (i), patterning is carried out with lithography.

The space at this time is good at the minimum spacing of a design rule, and does not need to take a doubling gap margin.

That is because the doubling gap margin can be substituted by a side wall.

And as shown in Fig. 4 (j), the polysilicon layer on the 2nd transistor Tr2 located about in the 1st transistor Tr1 field and on the 1st transistor Tr 1 is removed by RIE, and a resist layer is exfoliated.

Hereafter, the explanation progresses to processes, such as formation of a inbetween layers insulation layer.

[0031] Moreover, instead of the process of the Fig. 4 (i) and (j) mentioned above, for example as in Fig. 4 (h), you may be made to process the 3rd polysilicon layer 5, embedding for example, SiO, SOG, or a resist on a self-matching target as the mask material 2 into the slot made when the 3rd polysilicon layer 5 was formed, and using it as a mask.

[0032] Next, it considers how many memory transistors can be formed into the line/space of one unit as a result using Fig. 5 .

In addition, in Fig. 4 , L shows the minimum design rule, and since it is easy, it makes a line/space the length of 4L/4L.

Moreover, the thickness of ONO is ignored.

[0033] As shown in Fig. 5 (a), in the usual 1st polysilicon case, the number of memory transistors is one in a line / space 1 unit.

On the other hand, in this embodiment, as shown in Fig. 5 (b), four transistors of gate-length 2L are formed into 4L+4L=8L.

Specifically, one 1st transistor Tr1, two 2nd transistor Tr2, and one 3rd transistor Tr3 becomes a total of four pieces.

Consequently, according to this embodiment, the degree of integration can be increased to 4 times the usual.

[0034] As explained above, according to this example, after dwindling the gate of the 1st layer by the resist-ashing method and forming ONO layer, using MONOS as an element, since the transistor by the side wall is produced with the 2nd layer of 2nd polysilicon 4, ONO layer is formed further and the transistor is formed between the side walls in the 3rd layer of 3rd polysilicon layer 5, within the limits of present manipulation technique, the degree of integration of non-volatile memory can be improved.

Consequently, since the cost per bit can be reduced, there is an advantage which can lower

the price of a product.

Moreover, the side wall doubling gap margins can be absorbed, and a memory cell can be formed using the minimum manipulation dimension.

[0035] In addition, at this embodiment, although NAND type semiconductor nonvolatile storage was explained as an example, it cannot be overemphasized that it is not limited to this and this invention can be applied also to contact less type NOR semiconductor nonvolatile storage.

[0036]
[Effect of the Invention] As explained above, according to this invention, the degree of integration of non-volatile memory can be improved within the limits of present manipulation technique. Consequently, since the cost per bit can be reduced, there is an advantage which can lower the price of a product.

[Brief Description of the Drawings]
[Fig. 1] It is the cross section showing one example of NAND type semiconductor nonvolatile storage concerning this invention.
[Fig. 2] It is explanatory Fig. of ONO structure.
[Fig. 3] It is drawing for explaining the manufacture technique of the semiconductor nonvolatile storage of Fig. 1 .
[Fig. 4] It is drawing for explaining the manufacture technique of the semiconductor nonvolatile storage of Fig. 1 .
[Fig. 5] It is drawing for measuring and explaining the degree of integration with elegance this invention article and conventionally.
[Fig. 6] It is drawing for explaining NOR type memory cell.
[Fig. 7] It is drawing for explaining NAND type memory cell.

[Description of Notations]
Tr1 -- The 1st transistor
Tr2 -- The 2nd transistor
Tr3 -- The 3rd transistor
1 -- Semiconductor substrate
2 -- Gate insulator layer
3 -- The 1st polysilicon layer
4 -- The 2nd polysilicon layer
5 -- The 3rd polysilicon layer
6, 7 -- Between layer insulation layer